Generator provides 537 NTSC pattern

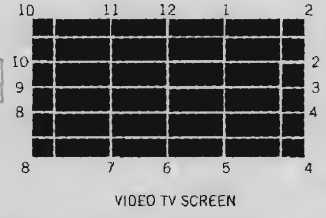
Adolfo Mondragon, Philips Components, Juarez, Mexico

If you're involved in the television, CRT, or deflection-yoke business, the circuit in **Figure 1** can prove useful for adjusting convergence and purity performance. The circuit generates dots, 537-line-crosshatch, and negative-field (crosshatch-inverted) patterns. You normally use the dots pattern to measure convergence performance using computer-camera equipment, such as the Minolta CC110. The crosshatch also measures convergence but on a visual basis only. The negative field is useful for adjusting and evaluating purity performance.

Much commercial equipment is available for pattern generation, but the patterns they generate are a mesh of approximately 16 horizontal×16 vertical lines—a lot of lines, when you need only a 535 mesh. In a factory where you must inspect 1000 TVs every day on the production line, a 16×16-line pattern is fatiguing and makes it difficult to concentrate on the critical specification points. All TV, CRT, and deflection-yoke manufacturers specify the convergence- tolerance limits in the intersection of the 535 lines at the edge of the screen. To identify the intersection points at the edges, the pattern in **Figure 2** uses "clock" numbers. The generator has the following characteristics:

- Its crosshatch pattern uses five vertical and seven horizontal lines.
- Its video synchronization uses a noninterlace mode.
- In noninterlace mode, its video signal requires no equalization pulses, thereby simplifying the circuit.
- Its 262 divider provides a simple way to generate the vertical-synchronization pulses.

Figure 2



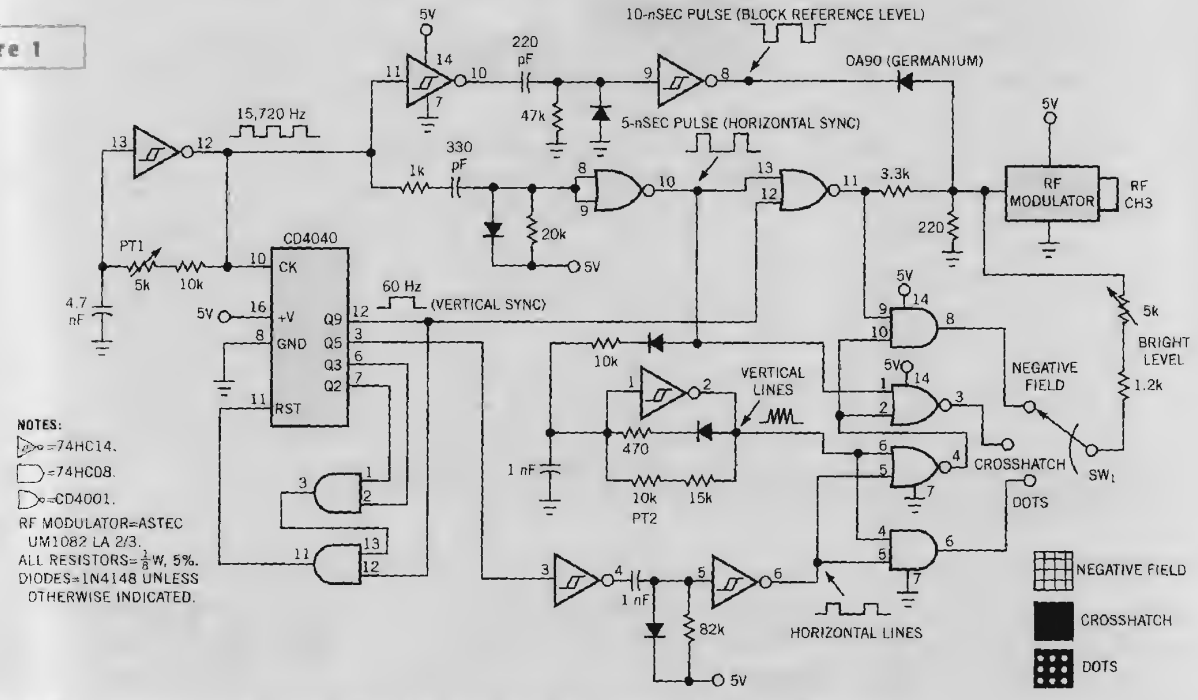
"Clock" numbers designate the edge intersection points in the crosshatch patterns that Figure 1's circuit generates.

Because modern TVs have excellent synchronization circuits, the horizontal oscillator requires no critical, expensive components. In fact, you can set the horizontal oscillator at 15.60 to 15.85 kHz, and the TV synchronizes.

The "brain" of the circuit is the 74HC14 Schmitt-trigger IC. The Schmitt triggers in **Figure 1** form both astable oscillators and monostable pulse shapers. The IC provides the 15.75-kHz master horizontal frequency, horizontal lines, and vertical lines. To adjust the circuit, trim PT1 to obtain a frequency that is as close as possible to 15.72 kHz. This frequency, rather than 15.75 kHz, provides a perfect 60-Hz (15,720÷262) vertical pulse. The CD4040 provides the divide-by-262 function. Adjust PT2 to obtain five pulses of 0.5 msec each. These pulses generate the vertical lines in the crosshatch pattern. (DI #2275).

To Vote For This Design, Circle No. 399

Figure 1



You can avoid the expense of a costly pattern generator by using this simple crosshatch- and dot-generator circuit.

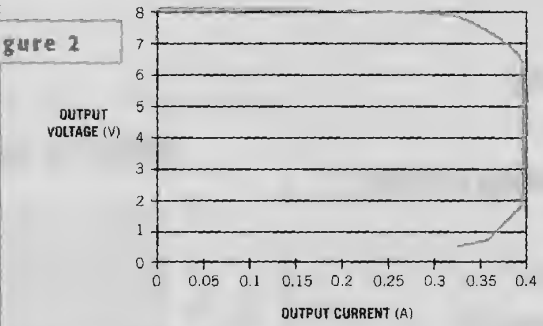
Offline IGBT charges batteries

Christophe Basso, Motorola SPS, Toulouse, France

POWER SUPPLIES FOR PORTABLE equipment must be light, and they must provide international travelers with a convenient universal input. Although switch-mode power supplies naturally benefit from a universal input, they are more expensive than standard linear supplies, which are based on a transformer. Recent insulated-gate bipolar transistors (IGBTs) offer an inexpensive way to charge batteries from the ac line. The MMG-05N60D in **Figure 1** sustains as much as 600V and has an avalanche characteristic comparable with that of a MOSFET having the same ratings. However, thanks to the IGBT's small die area, the device costs much less than the high-voltage MOSFET. Moreover, the MMG05N60D's SOT-223 package is pin- and size-compatible with the DPAK industry standard.

Figure 1's offline supply uses a current-mode technique, in which a discrete, double-bipolar thyristor (Q_1) forms a latch. You can use off-the-shelf components to generate the 50%-duty-cycle clock, provided that the components can generate a 50-kHz square wave using a low start-up current determined by R_3. This design uses a NAND-based Schmitt trigger, extracted from an MC14093. The IGBT's 7-nC gate charge lets you drive the device with simple logic gates. The IGBT receives its bias voltage through R_8, a 1-kΩ resistor. This resistor's relatively high value does not disturb the oscillator when the thyristor pulls the gate to ground. When the IGBT turns on, the primary current and the voltage across R_4 rise. When the peak current occurs, or when 700 mV appear on C_6, Q_1 turns on and cuts off the IGBT's conduction. As with any flyback circuit, the energy transfer charges C_1 and C_2, the output capacitors.

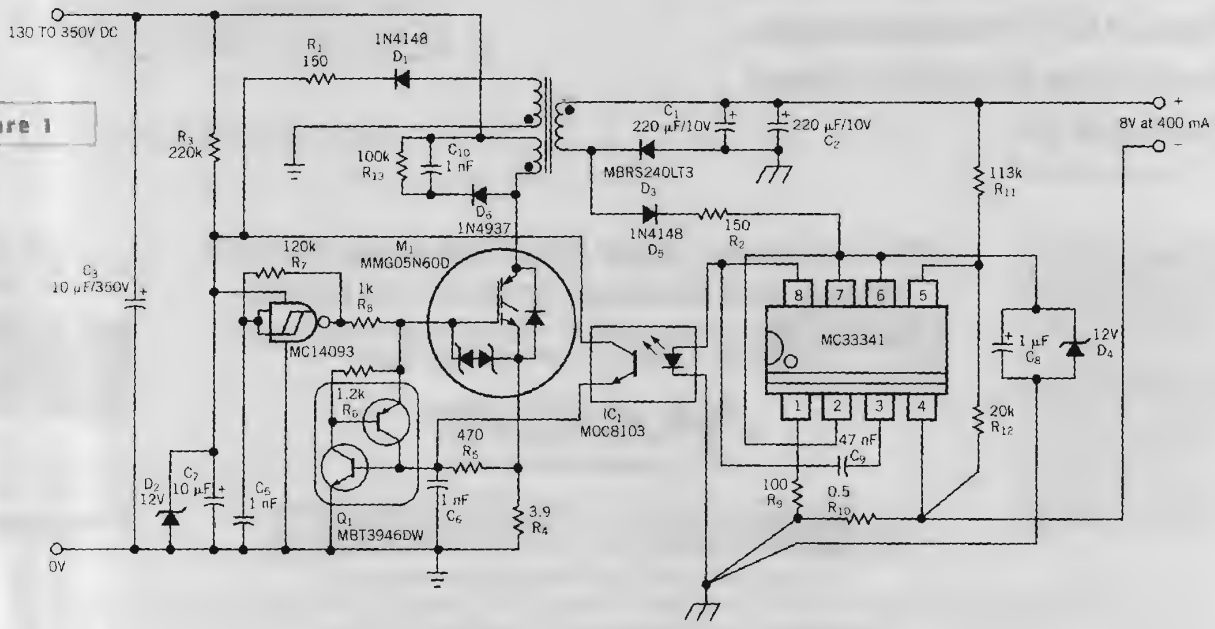
Figure 2



The MC33341 in Figure 1 provides a square I-V characteristic in Figure 1's battery charger.

In low-cost structures such as this one, you can easily control the output voltage and current by offsetting the dc level across C_6. The offsetting uses an optocoupler driven by a dedicated battery-charger circuit, the MC33341. This IC includes a dual control loop that regulates either the current (sensed by R_{10}) or the voltage (sensed by R_{11}/R_{12}). When the current is below its limit, the MC33341 regulates the output voltage at its nominal value (8V, for example) and allows the output current to increase. When the output current reaches the internal threshold ($0.2V/R_{10}$), the

Figure 1



An IGBT has a smaller die than does a MOSFET, cutting costs in a offline battery-charging applications.

current loop prompts the optocoupler to transform the supply into a constant-current source. **Figure 2** shows the supply's typical transfer function. You can download a Spice model of the MC33341 at http://mot2.indirect.com/models/bin/batmag_ic.html.

The dot-marked terminals of the transformer are wired in an unusual way. You use this atypical wiring technique because connecting a fully discharged battery can present a total short circuit at the output. If you short the output, the flyback auxiliary-winding voltage decreases, but the MC33341's supply disappears, leaving the supply without a current limit. To avoid this scenario, connect the output transformer so that it benefits from both the flyback and the forward voltage. When the output constrains the flyback voltage to a low value, the forward voltage powers the MC33341. The auxiliary winding also benefits from this structure. We tested the supply with a transformer having 6-mH primary inductance and auxiliary- and power-winding ratios of 0.12 and 0.06, respectively. To cancel any turn-on losses, you must prevent the supply from entering the continuous mode. The IGBT typically keeps the current-tail losses at 6 μJ (at I_C=0.3A, T_J=125°C, and dV_{CE}/dt=1 kV/μsec). (DI #2297).

To Vote For This Design,
Circle No. 400

MOS transistors form current-mode Schmitt trigger

Tai-Shan Liao, Chun-Ming Chang, and Wen-Yaw Chung, Chung-Yuan, Christian University, Taiwan, China

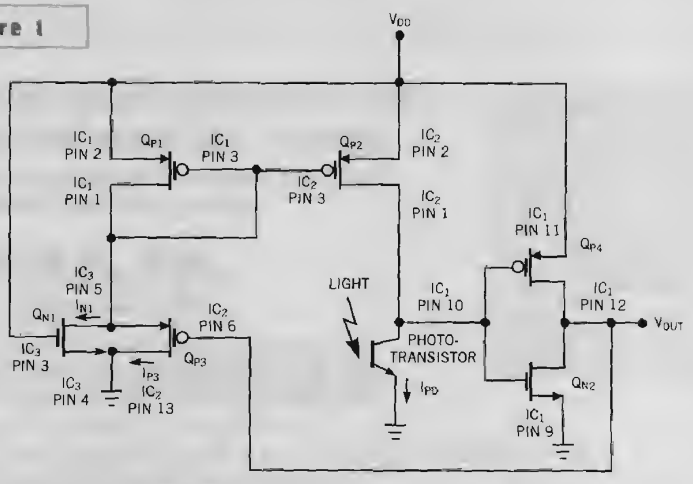
Schmitt triggers are useful in both analog and digital circuits for reducing sensitivity to noise and disturbances. Current-mode Schmitt triggers are particularly useful in photodetectors, barcode readers, and optical remote controls. The resistorless current-mode Schmitt trigger in **Figure 1** uses six MOS transistors. The circuit uses the output of an inverter and derives its feedback through a variation of threshold current. The circuit uses one inverter pair (Q_{N2}, Q_{P4}), one current-mirror pair (Q_{P1}, Q_{P2}), and two load devices (Q_{N1}, Q_{P3}). The gate of Q_{P3} receives feedback from the output of the inverter. The drain current of Q_{N1} is the lower threshold current (I_{TL}); the drain current of the Q_{N1}-Q_{P3} pair is the upper threshold current (I_{TH}). The hysteresis, I_H, is $I_{TH}-I_{TL}$, or $(I_{P3}+I_{N1})-I_{N1}=I_{P3}$.

The NMOS and PMOS transistors are components of three CD4007 ICs: IC_1, IC_2, and IC_3. The circuit operates as follows: First, assume that the output of the inverter is in its low state, turning Q_{P3} on. When the phototransistor current (I_{PD})exceeds the upper threshold (I_{TH}), the output of the inverter switches high, turning off Q_{P3}. When I_{PD} falls lower than the lower threshold current (I_{TL}), the inverter switches low, again turning on Q_{P3}. **Table 1** summarizes the relationships between V_{DD}, I_{TL}, I_{TH}, and I_H. The circuit in **Figure 1** can operate successfully from a 1.5V supply. (DI #2303).

TABLE 1–SCHMITT-TRIGGER THRESHOLDS AND HYSTERESIS

Power supply V_{DD} (V)	Upper limit I_{TH} (mA)	Lower limit I_{TL} (mA)	Hysteresis I_H (mA)
1.5	0.007	0.004	0.003
2	0.198	0.058	0.14
3	2.3	1.18	1.12
4.5	8.6	4.6	4
5	11.3	5.96	5.43
5.5	14.4	7.7	6.7
10	48.5	27.7	30.8
12	65	37.1	27.9
15	89	49	40

Figure 1



A Schmitt trigger provides hysteresis to this photodetector circuit to afford immunity to false triggering.

To Vote For This Design,
Circle No. 401

Eight-channel data-acquisition system features autocalibration

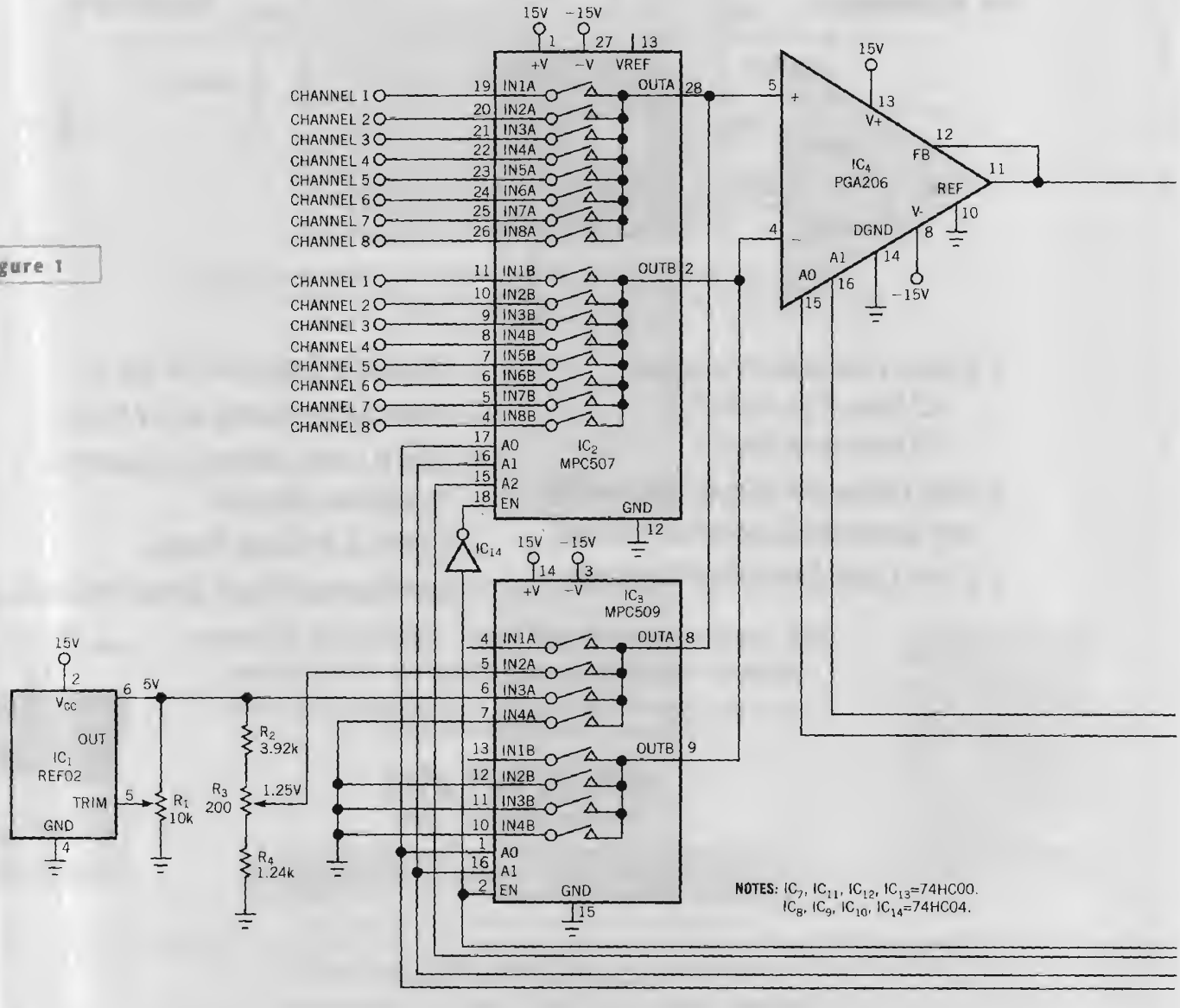
Mark Shill, Burr-Brown Corp, Tucson, AZ

THE CIRCUIT IN **Figure 1** is a versatile, eight-channel, differential-input, 16-bit data-acquisition system. A PC controls the circuit via the computer's parallel port. Under control of the PC, you can select one of eight differential voltage inputs, each with a programmable input-voltage range of ±1.25, ±2.5, ±5, or ±10V. In addition, calibration factors stored in the controlling PC's software calibrate each input range for gain and offset errors.

The heart of the system is the ADS7805 16-bit ADC. This ADC can digitize voltages of ±10V as fast as 100 kHz. A unique feature of the ADS7805 allows you to read its 16-bit output as a high byte and a low byte, selected by the Byte pin. When Byte is low, the upper byte of the conversion result is present at data-output pins

A PC calibrates gain and offset errors in a data-acquisition system by storing error-correction values collected through its parallel port.

Figure 1

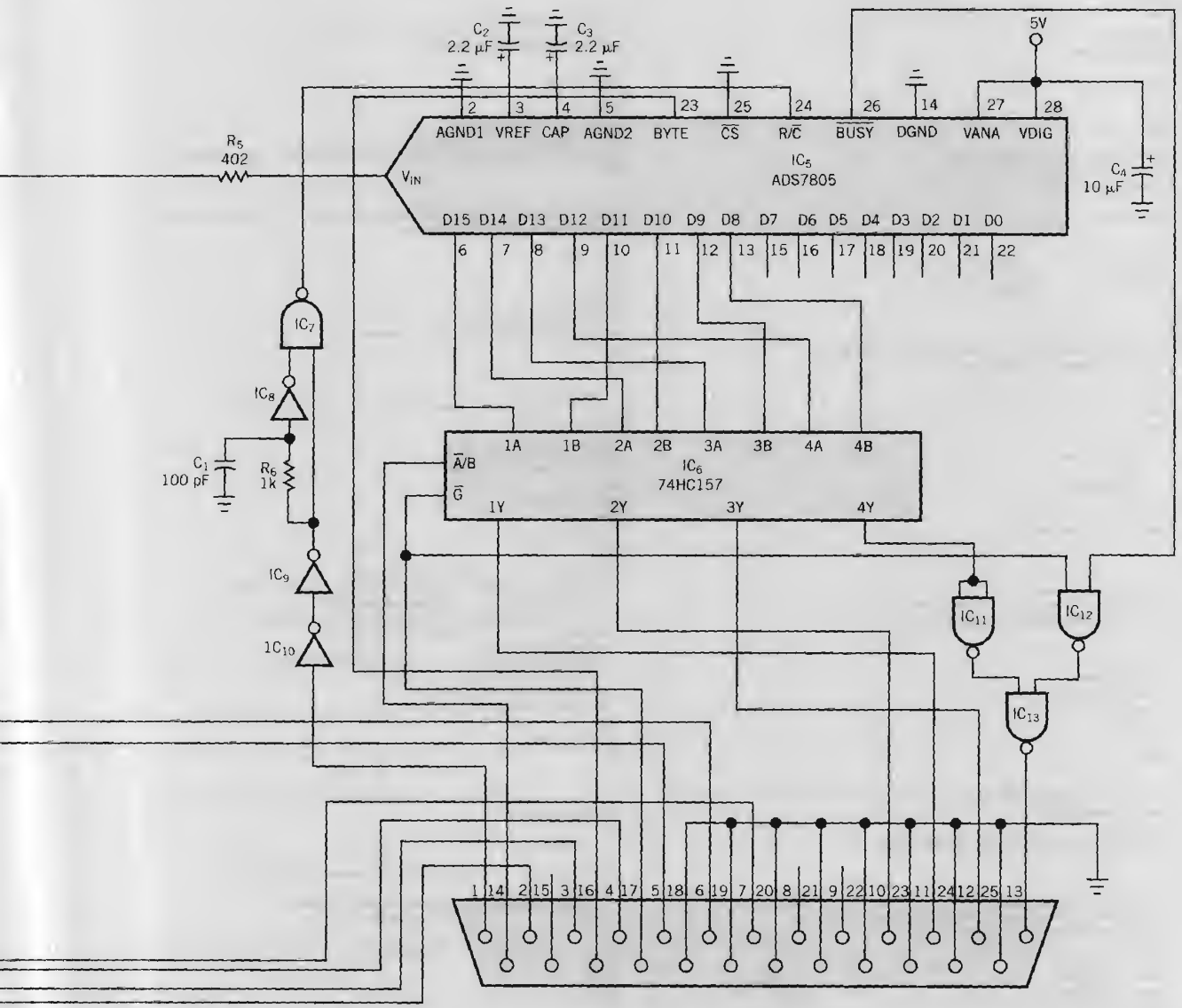


D15 through D8; when Byte is high, the lower byte appears. This feature simplifies the digital-data interface to the PC's parallel port, in that you need only one 74HC157 quad two-line-to-one-line multiplexer to convert the ADS7805's 16-bit digital data to four 4-bit nybbles. Logic gates IC_{11} through IC_{13} create an additional multiplexer channel for the PC to monitor the ADC's end-of-conversion signal $\overline{BUSY}$.

A short, active-low pulse applied to the R/$\overline{C}$ pin starts the conversion. Logic gates IC_7 through IC_{10}, with R_6 and C_1, generate the active-low pulse whenever –Strobe pin 1 of the PC's parallel port has a low-to-high transition. For the component values shown, the active-low pulse width is approximately 75 nsec. When the ADC finishes its conversion, which is signified by a low-to-high transition on $\overline{BUSY}$, you can read the 16-bit data results as four 4-bit words, under control of the PC's parallel-port output pins 14, 16, and 17 (**Table 1**).

IC_4 is a PGA206 digitally programmable-gain amplifier, which converts the selected differential-input voltage to a single-ended voltage output that connects to the ADS7805 through R_5. R_5 attenuates the ADC's input signal by approximately 1%, thus allowing the ADC to measure input voltages slightly beyond its normal ±10V input range. The DAC thus has a small overrange capability. The PC can select the PGA206's gain to be 1, 2, 4, or 8V/V, corresponding to input ranges of ±10, ±5, ±2.5, or ±1.25V, respectively. The parallel port's output pins 5 and 6 control the PGA206's address lines A0 and A1 to select the user-defined gain ranges.

IC_2, an MPC507 differential, eight-channel multiplexer, selects each of the eight input-voltage channels. Address lines A0, A1, and A2 select the active channel of the MPC507. These address lines connect to the parallel port's output pins 2, 3, and 4, respectively. A logic-high level on the multiplexer's EN pin enables the multiplexer. A logic-low level turns off the mulitplexer's outputs. The gain and offset



corresponding ADC input voltages are 5 and 10V for the gain ranges of 4 and 8V/V, respectively.

Offset calibration uses ground as the reference for each of the PGA206's gain ranges. IC_3 is a differential, four-channel analog multiplexer that switches in each of the calibration-voltage standards to the PGA206's inputs. Because each of the calibration-voltage standards is a known value, you can determine the system's gain and offset errors by digitizing each voltage standard and comparing the result to the theoretical value in the system's software. You can then store the resulting error-correction factors in a program array and use them to correct any measured input voltages in channels one through eight.

Listing 1 shows the Pascal program for the data-acquisition system. For simplicity, the **listing** shows the data-acquisition part of the program as a unit file, which links to the main program as shown. The program allows you to specify the number of ADS7805 readings to take to average the resulting measurements. A greater number of averages reduces the effects of any noise in either the input signal or the measurement system. The program variable Average sets the number of averages to take. If the input voltage exceeds the selected input-voltage range, the program signifies the overrange condition by writing "Overrange" to the display. You can download **Listing 1** from *EDN*'s Web site: www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2289. (DI #2289).

TABLE 1—PASCAL LISTING FOR AUTOCALIBRATED DATA-ACQUISITION SYSTEM

Parallel-port function	Parallel-port pin	Circuit function
– Strobe	1	ADS7805 convert
Data bit 0	2	Input multiplexer A0
Data bit 1	3	Input multiplexer A1
Data bit 2	4	Input multiplexer A2
Data bit 3	5	PGA206 A0
Data bit 4	6	PGA206 A1
Data bit 5	7	Input multiplexer enable
– Ack	10	Nybble bit 2
Busy	11	Nybble bit 3 (MSB)
PaperEnd	12	Nybble bit 1
Select	13	Nybble bit 0 (LSB)
– AutoLF	14	74HC157 – A/B
– Init	16	ADS7805 byte
– SelectIn	17	74HC157 enable
Ground	18 to 25	Ground

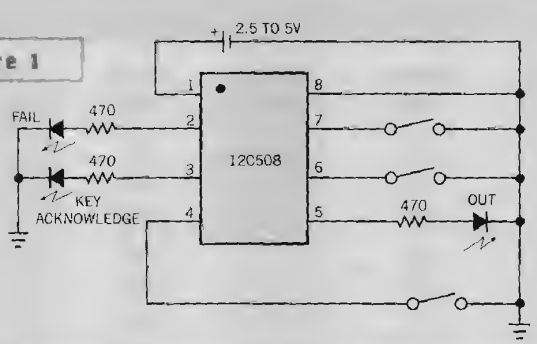
To Vote For This Design,
Circle No. 402

µC provides three-key, five-sequence lock function

William Grill, Riverhead Systems, Littleton, CO

Using MicroChip's 12-C508 eight-pin µC, you can inexpensively implement a digital-sequence lock with debounce and status-indicator features (**Figure 1**). The design exploits the internal-oscillator, watchdog-timer, and wake-up-on-pin-change features inherent in the µC, and it provides an application that supports key acknowledge and out-of-sequence error detection. The circuit debounces key entries and acknowledges them at Pin 3 with a short LED flash. The µC evaluates the entries against a sequence table that is internally coded to the defined sequence's length. At the end of the sequence, correctly sequenced inputs generate a 2-sec, high-true pulse on Pin 5; a wrong sequence, detected at any time during entry, generates a series of five flashing pulses on Pin 2.

Figure 1



An inexpensive µC implements a simple, foolproof digital-sequence lock with key debounce and status indication.

Using the watchdog-timer and wake-up-on-pin-change features to generate timing and initiate processing allows battery-powered operation. The µC also provides an auto-reset function after several seconds between expected entries. The lock-sequence's length and combination are coded characteristics that you establish during programming. Using only 150 bytes of code space, sequences longer than 100 steps are possible. You can also port the code to a larger 16C5x or 16C6x controller and take advantage of the opportunity to include embedded I/O or reporting functions, based on the correctly keyed access processes described here. You can download the assembly code for the PIC for the µC from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2299. (DI #2299).

To Vote For This Design,
Circle No. 403